



**ANNOTATED SPECIFICATION
PAGES**

1, 2, 7, and 14

for U.S. Patent Application No. 09/941,447

Attorney Docket No.: M-9999-1D US

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SEP - 9 2002
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FABRICATION OF
SEMICONDUCTOR STRUCTURES HAVING MULTIPLE CONDUCTIVE LAYERS
IN AN OPENING, AND METHODS FOR FABRICATING SAME



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BACKGROUND AND SUMMARY

The present invention relates to semiconductor technology.

Some embodiments of the invention facilitate creation of electromagnetic shielding for circuit nodes that carry AC (alternating current) signals. Such shielding advantageously reduces energy losses for the AC signals. The shielding also reduces noise in shielded regions.

Some embodiments allow fabrication of capacitors and capacitor networks in a small area.

According to some aspects of the invention, a circuit manufacturing method comprises:

forming an opening in a first side of a semiconductor substrate, with a plurality of conductive layers overlaying each other in the opening, the conductive layers including a first conductive layer and a second conductive layer overlaying the first conductive layer such that the first and second conductive layers ~~either~~ (i) are separated by an insulating layer in the opening, or (ii) form a P-N junction in the opening, or (iii) form a Schottky junction in the opening;

removing material from a second side of the semiconductor substrate to expose the second conductive layer in the opening on the second side of the substrate.

In some embodiments, the first and second conductive layers are separated by an insulating layer in the opening.

In some embodiments, the first conductive layer shields the substrate from AC signals carried by a contact pad made from the second conductive layer on a wafer

backside. Contact pads on the wafer backside can facilitate vertical integration and small scale packaging. See PCT publication WO 98/19337 (TruSi Technologies, LLC, 7 May 1998) and ^{U.S.} patent application no. 09/456,225 filed 6 December 1999 by O. Siniaguine ^{now U.S. Patent 6,322,903 documents} et al. Both of these applications are incorporated herein by reference.

5 In some embodiments, the first and second conductive layers provide conductive plates of a capacitor.

In some embodiments, the invention provides a circuit structure comprising a semiconductor substrate, an opening passing through the substrate between a first side of the substrate and a second side of the substrate, and a plurality of conductive layers which
 10 overlay sidewalls of the opening, wherein the conductive layers include a first conductive layer and a second conductive layer such that the first and second conductive layers either (i) are separated by an insulating layer in the opening, or (ii) form a P-N junction in the opening, or (iii) form a Schottky junction in the opening; wherein the second conductive layer is exposed on the second side of the opening, and the first conductive layer
 15 surrounds the second conductive layer in the opening.

In some embodiments, a circuit manufacturing method comprises:

forming an opening in a first side of a semiconductor substrate;

forming at least three conductive layers overlaying each other in the opening, such that each two consecutive conductive layers ~~either~~ (i) are separated by an insulating
 20 layer in the opening, or (ii) form a P-N junction in the opening, or (iii) form a Schottky junction in the opening;

removing material from a second side of the semiconductor substrate to expose at least one of said conductive layers in the opening on the second side of the substrate.

In some embodiments, a circuit structure comprises:

25 a semiconductor substrate, and an opening passing through the substrate between a first side of the substrate and a second side of the substrate;

at least three conductive layers overlying each other in the opening, such that each two adjacent conductive layers either (i) form a P-N junction in the opening, or (ii) form

We now describe particular materials and processing techniques used in some embodiments. Conductive layers 210, 320 can be made of metals, doped polysilicon, conductive metal silicides, and their combinations. Insulating layers 120, 310, 340 can be made of silicon dioxide, silicon nitride, silicon oxynitride, aluminum oxide, tantalum oxide, titanium oxide, and their combinations. Layers 210, 320, 120, 310 can be fabricated by known techniques, such as sputtering, thermal oxidation, or CVD (chemical vapor deposition). Other materials and fabrication techniques, known or to be invented, can also be used. Each of layers 210, 320, 120, 310, 340 can include multiple layers and multiple materials. In some embodiments, layer 210 includes a layer that has a higher conductivity than the adjacent semiconductor regions 110.1.

In some embodiments, the wafer thinning is a blanket etch process. When layers 210, 310 become exposed, the etch continues and etches the substrate 110 and the layers 210, 310 at the same time. In Fig. 4A, insulator 310 protrudes down after the etch from the backside surface of substrate 110. The protruding insulator ^{helps} helping insulate the substrate from contact pads 320C when the contact pads are bonded to a wiring substrate or another integrated circuit. Conductor 210 also protrudes down from substrate 110, but insulator 310 protrudes more to improve insulation between conductors 210, 320. This profile is achieved by choosing the materials and the etching process so that the etch rate of wafer 110 is higher than the etch rate of layer 210 and the etch rate of layer 210 is higher than the etch rate of insulator 310. The layer 320 has the lowest etch rate (zero for example). In some embodiments, the etch is performed by fluorine containing plasma at atmospheric pressure. A suitable etcher is type Tru-Etch 3000 (Trademark) available from Tru-Si Technologies, Inc., of Sunnyvale, California. Wafer 110 is made of monocrystalline silicon. Conductor 210 is made of titanium, tungsten, molybdenum, vanadium, or their silicides, or titanium nitride, or a combination of these materials. Insulator 310 is made of silicon dioxide, silicon nitride, silicon oxynitride, or a combination of these materials. Conductor 320 is formed, or includes a layer formed, of aluminum, copper, nickel, or a combination of these materials.

Fig. 5 illustrates another embodiment. The same etch is used as in Fig. 4A, but the conductor 210 is etched faster than substrate 110 and insulator 310. For example, the substrate 110 can be monocrystalline silicon and the layer 210 can be doped polysilicon. The remaining materials can be as in Fig. 4A. Polysilicon is initially etched faster than monocrystalline silicon 110, but when polysilicon becomes recessed relative to silicon

Fig. 22 is a circuit diagram for the structure of Fig. 16. Capacitor 1504.1 is formed by conductive layers 320, 210.2 and insulator 310.2. Capacitor 1504.2 formed by conductive layers 210.2, 210.1 and insulator 310.1. Capacitor 1504.3 is formed by layer 210.1, substrate region 110.1, and insulator 1110.

- 5 Any one or more of capacitors 1504.1, 1504.2, 1504.3 can be junction capacitors or rectifiers.

I_n

- The capacitor plates can be interconnected. Fig. 22, the layers 320, 210.1 are connected together, as shown by a line 1910, so that the capacitors 1504.1, 1504.2 are connected in parallel between contact pad 320C and conductor 210.2 which is connected to a circuit 1510. Connection 1910 can be made outside of the opening 130. Connection 1910 can be a permanent connection. Alternatively, connection 1910 can be programmable (e.g. using a fuse or an antifuse), to allow the capacitance to be adjusted during or after manufacturing. Connection 1910 can be realized by means of contact openings (not shown) etched outside of opening 130 and allowing the layers 320, 210.1 to contact each other directly or through some other layer or layers.

Any number of layers 210 can be used to form any number of capacitors and rectifiers between contact pad 320C and substrate 110 and to provide desired electromagnetic shielding. Connections 1910 can be used to obtain a desired network.

- Fig. 23A illustrates another type of capacitor structure. The structure is manufactured as follows:

1. One or more openings 130 are formed in the front side of substrate 110, as in Figs. 1-17.
2. Optionally, insulating layer 1110 is formed as in Fig. 16.
3. One or more conductive layers 210 are formed in the openings as in Fig. 15 or 16. Only one such layer is shown in Fig. 23A. Insulating layers 310 (such as 310.1, 310.2 in Fig. 16) can optionally be formed between layers 210.
4. Optionally, insulator 310 is formed in the opening over the layers 210, using the same techniques as in Fig. 15.